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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/928,011	SEDLAK ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 8 is pending.

2. The office acknowledges the following papers:

Claims and arguments filed 2/27/2007.

Withdrawn objections and rejections:

3. The drawing objection has been withdrawn due to amendment.

New Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 8 recites "an adding unit ..." and "a subtracting unit ..." The claims do not specify that these units are separate units or a combined unit since subtraction and addition are one and the same that operate on different data. The applicants pointed out support within the specification that the adding and subtracting units are in a single device. However, no support within the specification has been found that details the

adding and subtracting unit being separate units. Thus, the claim doesn't have written description support of the claimed invention without stating that the adding unit and subtracting unit is within a single device.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 8 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites "an adding unit ..." and "a subtracting unit ..." It's unclear if both the adding unit and the subtracting unit are separate units or a combined unit since subtraction and addition are one and the same that operate on different data. The applicant pointed out support within the specification that the adding and subtracting units are in a single device. However, no support within the specification has been found that details the adding and subtracting unit being separate units. For examination purposes, these two units will be interpreted as a single device.

New Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goetz (U.S. 5,854,913), in view of Yoshida (U.S. 5,088,030), in view of May et al. ("The PowerPC Architecture"), in view of K. Short ("Embedded Microprocessor Systems Design"), and in view of Kanzaki (U.S. 5,983,018).

10. As per claim 8:

Goetz discloses a microprocessor for processing various assembler codes, comprising:

Depending on how the parameter is set, a different relative addressing takes place: (Relative addressing is defined as, "An addressing mode in which the effective address is formed by adding an offset to the program counter (or a portion thereof) during execution." (The Authoritative Dictionary of IEEE Standards Terms) Therefore, incrementing a program counter is relative addressing, because the program counter has a current value, and a new value is reached by adding an instruction length to the current PC address. Since the Q-bit indicates different instruction lengths to be added to the current PC address, different relative addressing takes place dependent on the Q-bit (Figure 9, Column 16, lines 47-64). Column

A program counter (NIFA Compute 807, figure 9 and column 16, lines 47-64)

A computation unit for computing relative addresses: (NIFA Compute 807, figure 9 and column16, lines 47-64)

While Goetz teaches multiple instruction sets being implemented and indicated by a parameter, Goetz is silent on how the different offsets for branch instructions are handled. It is well known in the art that PowerPC branch instructions add an offset to

the address of the branch instruction (May: Page 36, numeral 1), while x86 branch instructions add an offset to the address of the instruction following the branch instruction (Short: page 190, 2nd paragraph).

Goetz fails to teach a multiplexer having a first input, a second input for receiving a 0 value, and a third input receiving a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place; an addition unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input for an instruction length, and an output connected to said computation unit; a subtracting unit connected between said program counter and said computation unit for the relative addresses, said subtracting unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit; and a memory for storing an instruction length and having an output connected to said first input of said multiplexer.

However, Yoshida disclosed hardware to implement an x86-like branch instruction, which adds an offset to the address of the instruction following the branch instruction:

A program counter (Yoshida: Figure 2 element 13, column 3 lines 32-38);

A computation unit for computing relative addresses (Yoshida: Figure 2 element 17, column 3 lines 45-56)(The displacement is the offset that is added to the program counter output from the first adder.);

An adding unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input and an output connected to said computation unit (Yoshida: Figure 2 element 15, column 3 lines 39-44)(The first adder has a first input from element 13, which stores the PC. The first adder also has a second input that is the word length of the current instruction. The output of the first goes to the second adder that computes relative addresses for branch instructions.);

A subtracting unit connected between said program counter and said computation unit for the relative addresses, said subtracting unit having a first input connected to said program counter, a second input, and an output connected to said computation unit (Yoshida: Figure 2 element 15, column 3 lines 39-44)(The first adder has a first input from element 13, which stores the PC. The first adder also has a second input that is the word length of the current instruction. The output of the first goes to the second adder that computes relative addresses for branch instructions. It is inherent that a binary adder is also a subtraction unit if the binary inputs are in two's complement form, because there is no difference in hardware between adding two's complement numbers and subtracting two's complement numbers. A two's complement adder is inherently a subtraction unit as well.);

A memory for storing an instruction length and having an output connected to said first input of said multiplexer (Yoshida: Figure 2, column 4 lines 1-7)(The word length is decoded from the instruction. Therefore, the word length is part of the

instruction that is stored in memory. Thus, the memory storing the instruction stores the word length that is inputted to the first adder.).

The processor of Goetz contains instruction sets and their equivalent pipelines for x86 and Power PC instructions. Goetz is silent on how to implement the PC computations for x86 instructions. One of ordinary skill in the art would have been motivated by this to find Yoshida that implements PC calculations through two adders. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the PC calculations of Yoshida into the processor of Goetz.

Goetz and Yoshida failed to teach a multiplexer having a first input, a second input for receiving a 0 value, and a third input receiving a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place; an addition unit having a second input connected to said multiplexer and a third input receiving the parameter; and a subtracting unit having a second input connected to said multiplexer and a third input receiving the parameter.

However, May disclosed a multiplexer having a first input, a second input for receiving a 0 value, and a third input receiving a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place (May: Page 36 number 1)(May disclosed that Power PC instructions use the branch instruction address instead of the next PC that Yoshida uses. One of ordinary skill in the art would have realized that a MUX would need to be used to accommodate both types of calculations. A zero would be added with the current PC for Power PC branch instructions and the instruction length of Yoshida

would be added to the current PC for all other instructions. It's obvious to one of ordinary skill in the art that when a Power PC branch instruction is decoded, a control signal would control the MUX to select the zero value instead of the instruction length value.).

An addition unit having a second input connected to said multiplexer (May: Page 36 number 1)(May disclosed that Power PC instructions use the branch instruction address instead of the next PC that Yoshida uses. One of ordinary skill in the art would have realized that a MUX would need to be used to accommodate both types of calculations. A zero would be added with the current PC for Power PC branch instructions and the instruction length of Yoshida would be added to the current PC for all other instructions. It's obvious to one of ordinary skill in the art that when a Power PC branch instruction is decoded, a control signal would control the MUX to select the zero value instead of the instruction length value. The output of the MUX is sent to the adder/subtracter unit.); and

A subtracting unit having a second input connected to said multiplexer (May: Page 36 number 1)(May disclosed that Power PC instructions use the branch instruction address instead of the next PC that Yoshida uses. One of ordinary skill in the art would have realized that a MUX would need to be used to accommodate both types of calculations. A zero would be added with the current PC for Power PC branch instructions and the instruction length of Yoshida would be added to the current PC for all other instructions. It's obvious to one of ordinary skill in the art that when a Power PC branch instruction is decoded, a control signal would control the MUX to select the

zero value instead of the instruction length value. The output of the MUX is sent to the adder/subtracter unit.).

Goetz and Yoshida are both silent as how to correctly calculate a branch target address. May disclosed that the current PC value is used to add the branch displacement instead of the next PC. One of ordinary skill in the art would have been motivated to find out how to correctly calculate branch instructions in order to correctly calculate the branch target address to ensure valid program results. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the teachings of May into the processor of Goetz and Yoshida.

Goetz, Yoshida, and May failed to teach an addition unit having a third input receiving the parameter; and a subtracting unit having a third input receiving the parameter.

However, Kanzaki disclosed an addition unit having a third input receiving the parameter (Kanzaki: Figure 6 elements 43-44, column 6 lines 31-48)(Yoshida: Figure 2 element 15)(Elements 43-44 tells if the flag is set from an instruction that requires the PC be decremented. When combined with Yoshida, this element tells the first adder of Yoshida when an exception occurred that requires a subtraction to get the original PC of the offending instruction. When a subtraction isn't required, the first adder operates normally as described by Yoshida.); and

A subtracting unit having a third input receiving the parameter (Kanzaki: Figure 6 elements 43-44, column 6 lines 31-48)(Yoshida: Figure 2 element 15)(Elements 43-44 tells if the flag is set from an instruction that requires the PC be decremented. When

combined with Yoshida, this element tells the first adder of Yoshida when an exception occurred that requires a subtraction to get the original PC of the offending instruction. When a subtraction isn't required, the first adder operates normally as described by Yoshida.).

Yoshida disclosed a method of generating the next PC for a next instruction to be fetched from the instruction cache. Yoshida failed to teach interrupt and exception handling. One of ordinary skill in the art would have been motivated to include interrupt and exception handling within the processor of Yoshida and Goetz to allow for corrective action when a problem occurs in the processing of instructions. Therefore, one of ordinary skill in the art would have been motivated to find how to handle interrupts and exceptions to add the functionality of Kanzaki to correctly point to the offending instruction when an interrupt is finished. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the interrupt handling method of Kanzaki to insure that the correct program counter will be used once execution is restarted.

Response to Arguments

11. The arguments presented by Applicant in the response, received on 2/27/2007 are partially considered persuasive.

12. Applicant argues "Goetz, Yoshida, May, and Short failed to teach a adding unit and a subtracting unit in the same device."

This argument is not found to be persuasive for the following reason. An adder and a subtraction unit are one in the same. Both devices in a processor perform additions, with the subtraction unit performing an addition on a two's complement number.

13. Applicant argues "Goetz, Yoshida, May, and Short failed to teach a adding unit and a subtracting unit in the same device receiving a parameter designating a respective assembler code."

This argument is found to be persuasive for the following reason. The examiner agrees that the references failed to teach this because the references failed to teach an instance where an PC would be decremented. However, a new ground of rejection has been given due to the amendment.

14. Applicant states "The claims require two separate units for addition and subtraction to the program counter."

This argument is not found to be persuasive for the following reason. The claims don't state that the adding unit and the subtraction unit have to be separate entities. Thus, the claims can be interpreted as a single device, which is described in the fourth embodiment of the application. The examiner notes that the applicant provided no support within the specification for having separate adding and subtraction units. The drawings also do not show the invention containing a separate addition and subtraction unit within the same figure.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

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